Review Approval

Prepare Request
Search Requests
Generate Reports
Approvals
Help
　Wizard

Search Requests
New Search
Refine Search
Search Results

Clone Request
Edit Request
Cancel Request

Search Detail

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For Review and Approval process questions please contact the **Application Process Owner**

1 of 1   1/2/2008 2:38 PM

Completing the Journey of Moore's Law

Presentation at Notre Dame

May 4, 2004
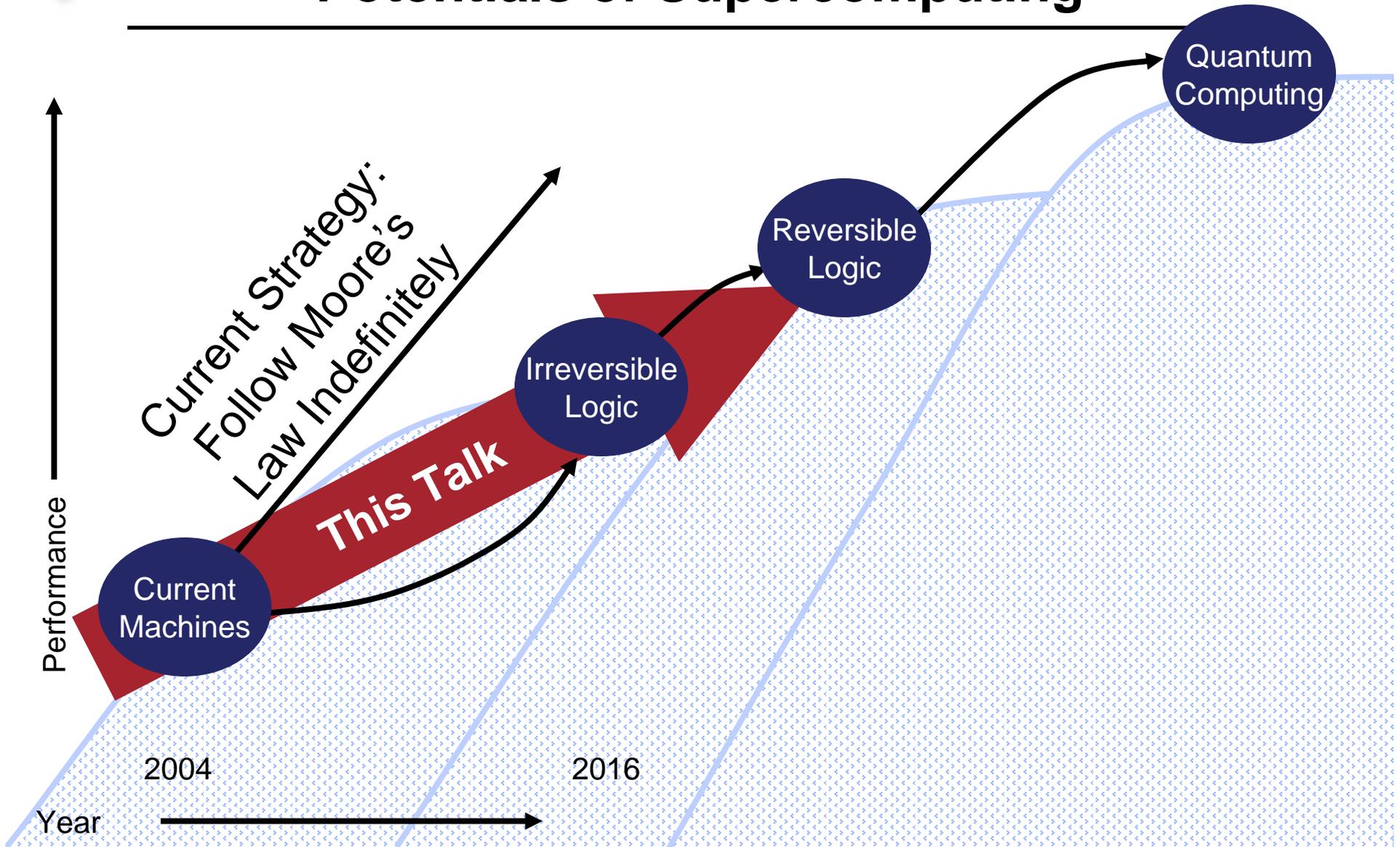
Erik P. DeBenedictis

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Potentials of Supercomputing

Outline

- **Applications of the Future**
- **Limits of Moore's Law**
- **How to Reach the Limit**
  - **Aerogel model**
  - **Applications Modeling**
- **No Need For a Breakthrough**
- **Architecture**
- **Beyond Moore's Law**

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# Simulation of Physics on a Computer

- **Space is divided into cells, each with computer variables representing the physical state of the volume represented by the cell**
- **The computer updates the state of a cell for successive time intervals ΔT based on some physical laws**
- **I. e. $S_{ijk}' = f(S_{ijk},$ states of nearby cells)**

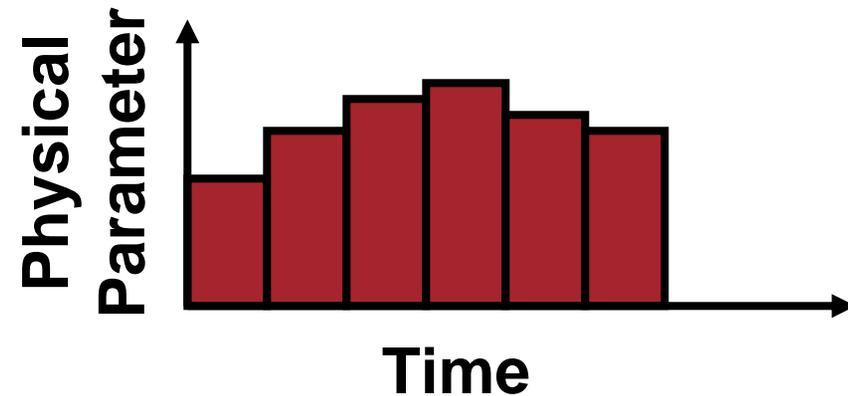S_{ijk}

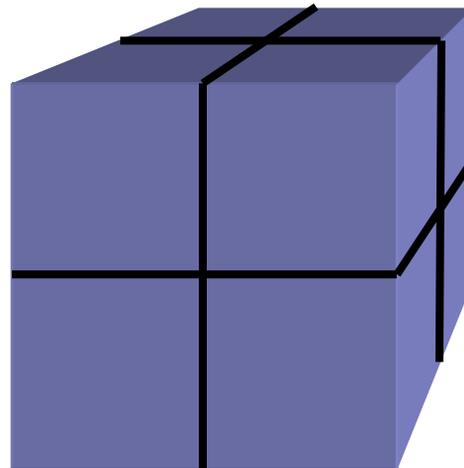Cell with "state" of space
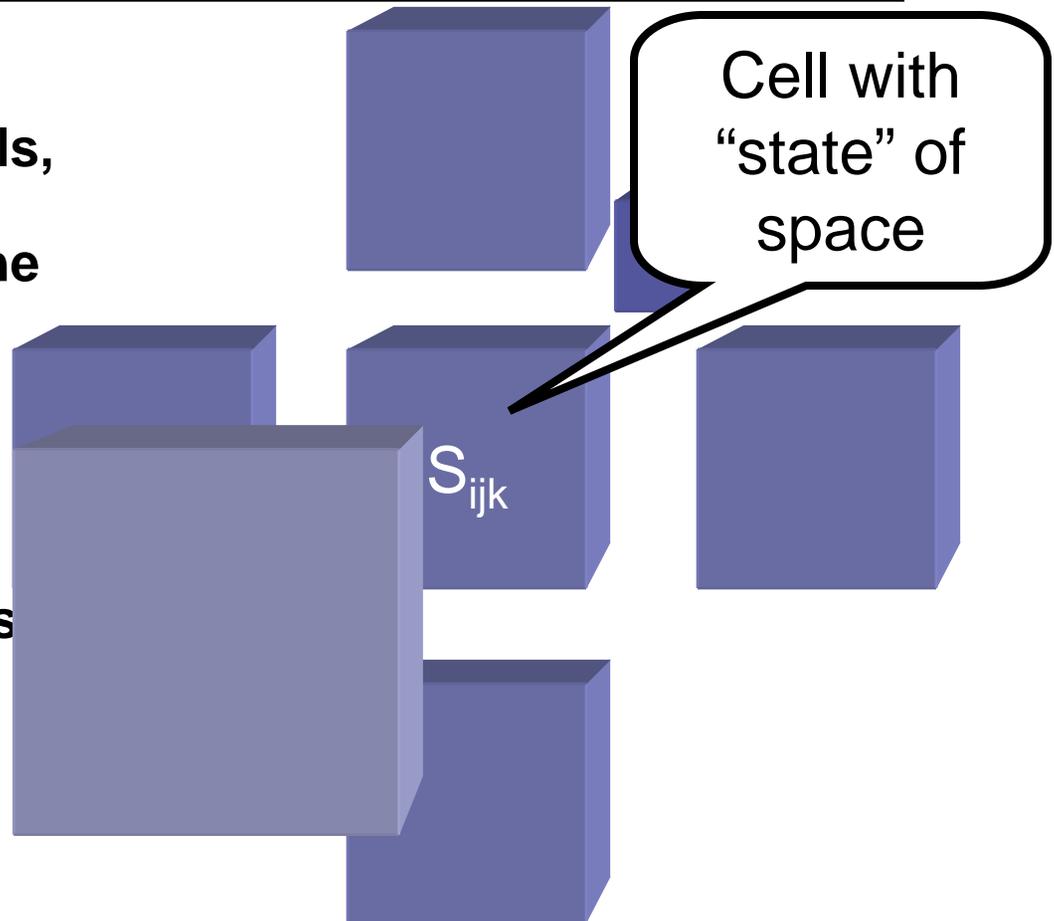
Fourth Power Scaling Rule

Reference
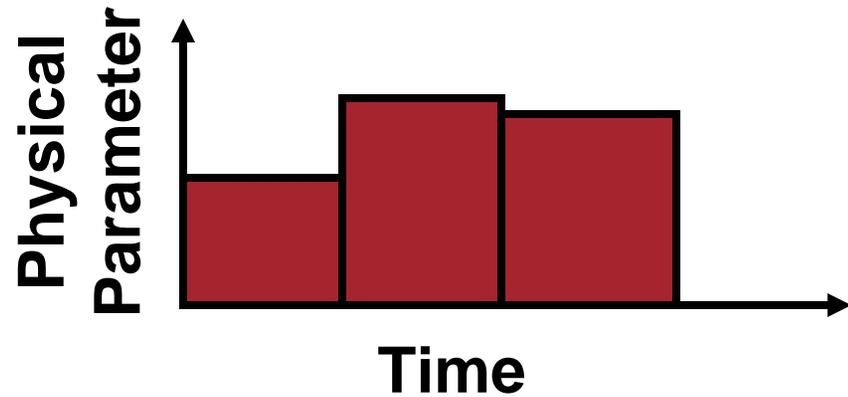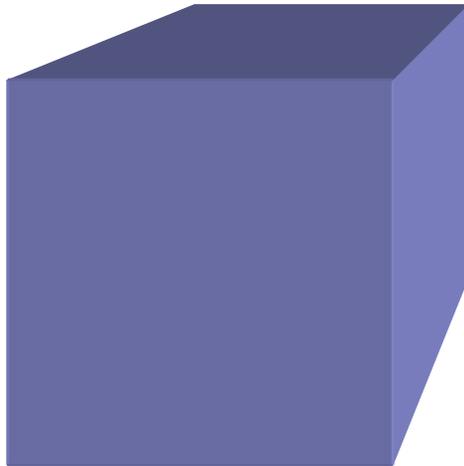
2× spatial resolution, 2× time steps → $2^4×$ FLOPS

Example: Earthquake Risk Mitigation

- **In an Earthquake-prone region**
  - Some areas the size of city blocks shake a lot
  - Others are stable

- **This effect is due to focusing or deflection of seismic waves due to underground rock structure**

- **Mitigation**
  - Identify dangerous areas and avoid building there
  - Identify dangerous areas by simulating many typical Earthquakes and noting the shaking
  - Requires an image of the underground rock structure

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Example Application: Earthquake Mitigation

- **Forward simulation**
  - **Match the results of a seismic simulation with observed data from seismographs**
- **Imaging**
  - **Deduce the structure of rock under the region (imaging) by repeatedly simulating the error from forward simulation by adjoint methods**
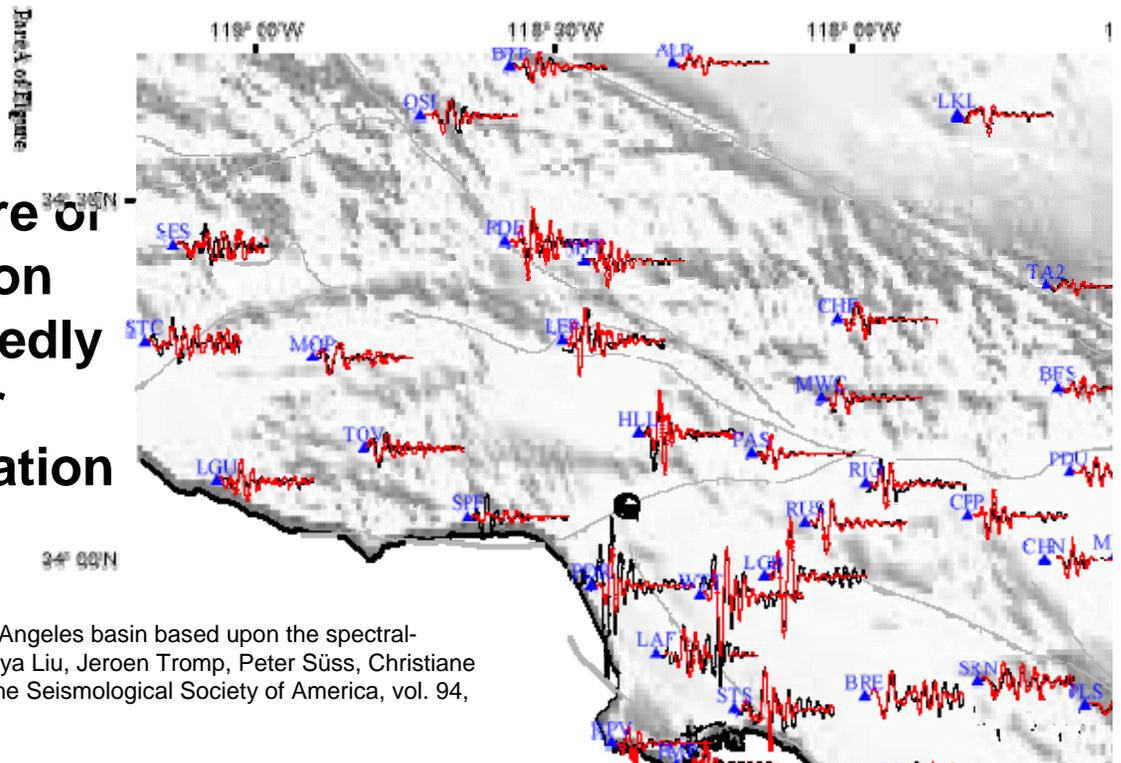
Simulations of ground motion in the Los Angeles basin based upon the spectral-element method, Dimitri Komatitsch, Qinya Liu, Jeroen Tromp, Peter Süss, Christiane Stidham and John H. Shaw, Bulletin of the Seismological Society of America, vol. 94, number 1, in press (2004)

Example: Earthquake Risk Mitigation

- **Today**
  - **Codes run at Caltech, Pittsburgh Supercomputer**
  - **Uses frequencies to 1 Hz, or a wavelength or several miles in rock**
  - **Computers are about 5 Teraflops**

- **Limit**
  - **Seismographs collect data to 20 Hz or more, or hundreds of feet in rock**
  - **Buildings are hundreds of feet in size, so this is useful resolution**
  - **Required computer 5 Teraflops $\times 20^4 = 1$ Exaflops**

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Earthquake Risk Mitigation

- **Algorithms: Written**

- **Code: Runs**

- **Input Data: Exists**

- **Consequence of Not Proceeding: People Die**

- **Required FLOPS: 1E = 1000P = 1,000,000T**
  - **25,000 $\times$ Earth Simulator**

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Global Climate

- **Objective**
  - **Collect data about Earth**
  - **Model climate into the future**
  - **Provide "decision support" and ability to "mitigate"**
- **Approaches**
  - **Climate models exist, but need they more resolution, better physics, and better initial conditions (observations of the Earth)**
- **Computer Resources Required**
  - **Increments over current workstation on next slide**

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FLOPS Increases for Global Climate

	Issue	Motivation
1 Zetaflops	Ensembles, scenarios $10\times$	Range of model variability
100 Exaflops	Run length $100\times$	Long-term implications
1 Exaflops	New parameterizations $100\times$	Upgrade to "better" science
10 Petaflops	Model Completeness $100\times$	Add "new" science
100 Teraflops	Spatial Resolution $10^4\times$ ($10^3\times$-$10^5\times$)	Provide regional details
10 Gigaflops	Current	

High-End Computing in Climate Modeling, Robert C. Malone, LANL, John B. Drake, ORNL, Philip W. Jones, LANL, and Douglas A. Rotman, LLNL (2004)

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Outline

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- **Limits of Moore's Law**
- **How to Reach the Limit**
  - **Aerogel model**
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- **No Need For a Breakthrough**
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*** **This is a Preview** ***

Best-Case Logic	Microprocessor Architecture	Physical Factor	Source of Authority
2.5×10^{26} ops/s		Landauer limit $500KW/(k_B T \log_e 2)$	Esteemed physicists
		Derate 20,000 convert logic ops to floating point	Properties of double precision floating point
12.5 Zetaflops		Derate limit 150 to achieve e^{-100} error rate	Current logic circuit properties
100 Exaflops	800 Petaflops	Derate for manufacturing margin (4×)	Estimate
25 Exaflops	200 Petaflops	Uncertainty (6×)	Gap in chart
4 Exaflops	32 Petaflops	Improved devices (4×)	Estimate
1 Exaflops	8 Petaflops	Projected ITRS improvement to 22 nm (100×)	ITRS committee of experts
	80 Teraflops	Lower supply voltage (2×)	ITRS committee of experts
	40 Teraflops	Red Storm	contract

Expert Opinion

Estimate

Assumption: Supercomputer consumes 2 MW wall power = 500 KW to chips
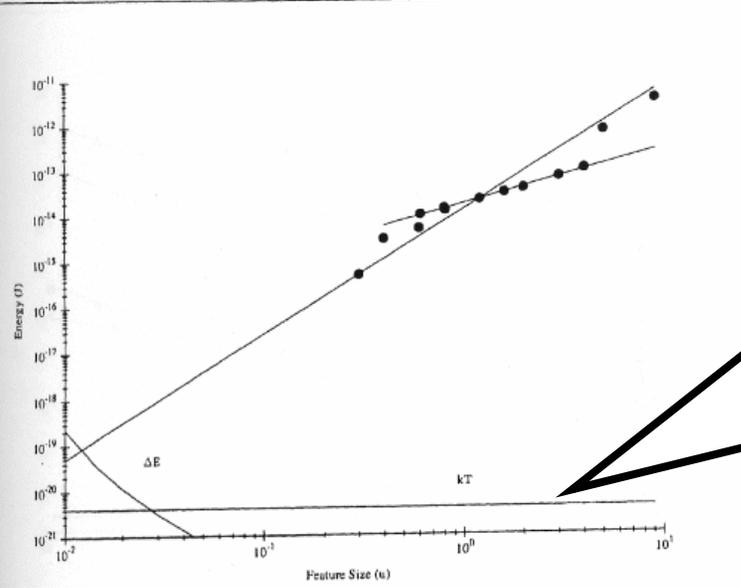
Thermal Noise Limit

This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function.
– R. Landauer 1961

kT "helper line," drawn out of the reader's focus because it wasn't important at the time of writing
– Carver Mead, Scaling of MOS Technology, 1994

SCALING OF MOS TECHNOLOGY 97

Energy (J)

ΔE

kT

Feature Size (u)

Metaphor to FM Radio on Trip to Chicago

- **You drive to Chicago listening to FM radio**
- **Music clear for a while, but noise creeps in and then overtakes music**
- **Why?**
  - **Signal at antenna weakens**
  - **Thermal electron noise constant at $k_B T$**

- **Analogy: You live out the next dozen years buying PCs every couple years**
- **Electrical effect**
  - **Moore's Law causes switching energy of gates to decrease at about 30% per year**
  - **Thermal electron noise constant at $k_B T$**

Details: Erik DeBenedictis, "Taking ASCI Supercomputing to the End Game," SAND2004-0959

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FM Radio and End of Moore's Law

Distance
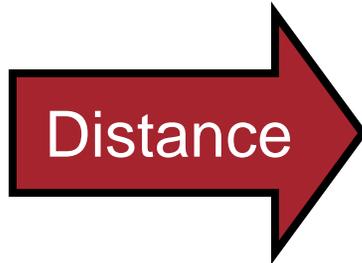
Driving away from FM transmitter→less signal
Noise from electrons → no change

Shrink
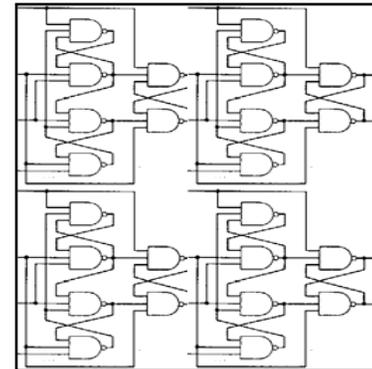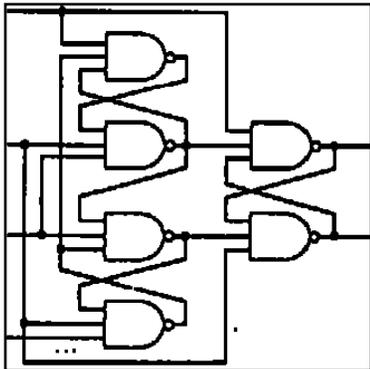
Increasing numbers of gates→less signal power
Noise from electrons → no change

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Amount of Reliability Needed

- **We expect computers to be reliable**
- **A future supercomputer will perform 10^{30}-10^{40} operations in its lifetime**
- **Error rate should be $< 10^{-30}$ - 10^{-40}**
- **Reliability due to thermal noise about $e^{-E/kt}$**
- **Need about e^{-100} error rate, or 100 $k_B T$ switching energy**

SNR (db)	Power Ratio	P_{error}
10	10	3.9×10^{-6}
14	25	6.8×10^{-13}
18	63	1.4×10^{-29}
22	160	3.3×10^{-71}
26	400	1.8×10^{-175}
30	1,000	4.5×10^{-437}
34	2,500	7.1×10^{-1094}
38	6,300	2.2×10^{-2743}
42	16,000	1.8×10^{-6886}
46	40,000	3.8×10^{-17293}
50	100,000	3.2×10^{-43433}
54	250,000	8.1×10^{-10194}
58	630,000	1.8×10^{-274025}
62	1,500,000	9.6×10^{-688315}

Noise Limit → (SNR 22)

2016 → (SNR 30)

Today → (SNR 50)

$$q := \int_t^\infty \frac{1}{\sqrt{2\pi}} e^{-\frac{x^2}{2}} dx; \quad t \to \sqrt{2 * 10^{\frac{snr}{10}}}$$

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Noise Levels

- 0 db Limit of hearing
- 20 db Rustling leaves
- 40-50 db Typical neighborhood
- 60-70 db Normal conversation
- 80 db Telephone dial tone
- 85 db City traffic inside car
- 90 db Train whistle @500'
- 95 db Subway train @200'
- 90-95 db Ear damage

- Today: 50 db
  - Thermal noise:Logic:: Rustling leaves:Talking
- 2016: 30 db
  - Thermal noise:Logic:: Talking:Train Whistle
- Reliability limit 20 db
 - Thermal noise:Logic:: Outside neighborhood:Talking

Personal Observational Evidence

- **Have radios become better able to receive distant stations over the last few decades with a rate of improvement similar to Moore's Law?**

- **You judge from your experience, but the answer should be that they have not.**

- **Therefore, electrical noise does not scale with Moore's Law.**

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SIA Semiconductor Roadmap

- **Generalization of Moore's Law**
  - **Projects many parameters**
  - **Years through 2016**
  - **Includes justification**
  - **Panel of experts**
    - **known to be wrong**
  - **Size between Albuquerque white and yellow pages**
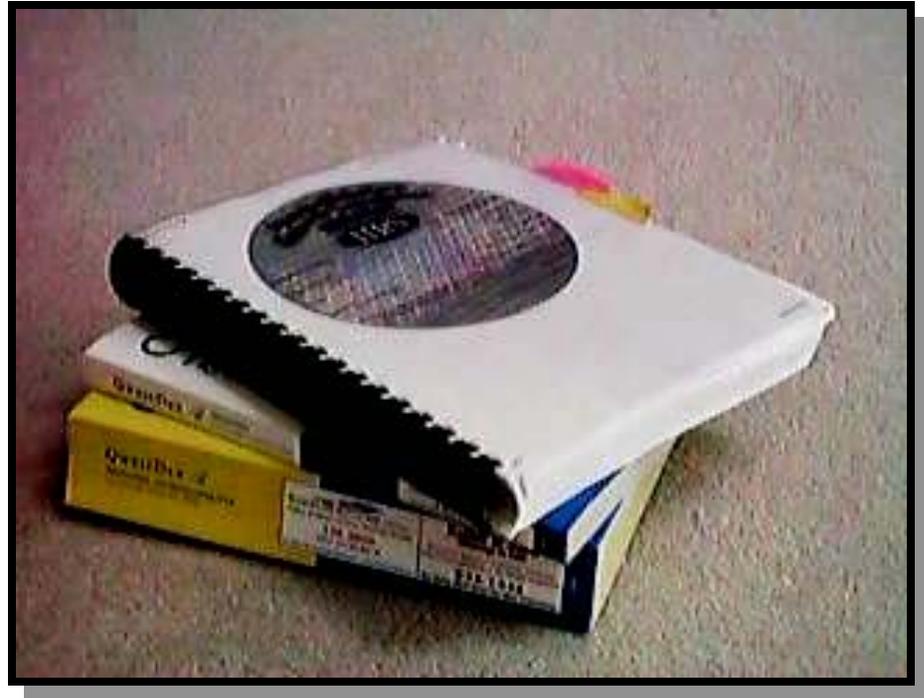
International Technology Roadmap for Semiconductors (ITRS), see http://public.itrs.net

Semiconductor Roadmap

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU / ASIC ½ Pitch (nm)	50	35	25
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Physical gate length high-performance (HP) (nm) [1]	18	13	9
Equivalent physical oxide thickness for high-performance T_{ox} (EOT) (nm) [2]	0.5-0.8	0.4-0.6	0.4-0.5
Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.5	0.5	0.5
T_{ox} electrical equivalent (nm) [4]	1.2	1.0	0.9
Nominal power supply voltage (V_{dd}) (V) [5]	0.6	0.5	0.4
Nominal high-performance NMOS sub threshold leakage current, $I_{sd,leak}$ (at 25°C) (µA/µm) [6]	3	7	10
Nominal high-performance NMOS saturation drive current, I_{on} (at V_{dd} at 25°C) (µA/µm) [7]	1200	1500	1500
Required percent current-drive "mobility/transconductance improvement" [8]	30%	70%	100%
Parasitic source/drain resistance (Rsd) (ohm·µm) [9]	110	90	80
Parasitic source/drain resistance (Rsd) pe...	25%	30%	35%
Parasitic capacitance percent of ideal gate...	31%	38%	42%
High-performance NMOS device τ (C_{gate} * V_{dd}/...) [11]	0.39	0.22	0.15
Relative device performance [12]	4.5	7.2	10.7
Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(l*L_{gate})*V^2) (fJ/Device) [14]	0.015	0.007	0.002
Static power dissipation per (W/Lgate=3) device (Watts/Device) [13]	9.7E-08	1.4E-07	1.1E-07

1,000 k_BT/transistor

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

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Limits for a Red Storm-Sized Computer

Best-Case Logic	Microprocessor Architecture	Physical Factor	Source of Authority
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Outline

- **Applications of the Future**
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- **No Need For a Breakthrough**
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Can We Reach the Limit?

- **Method: Compare modeled running time on perfect computer to real computer**
- **Application: Local calculations with global time step (SOR)**
- **Technology comparison:**
  - **22 nm transistors with 3D atom-by-atom assembly**
  - **Our best shot at an architecture**
- **Definition of Success: Our best shot comes within a constant factor of the theoretical peak**

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Aerogel Computer

- **Devise algorithm for a hypothetical aerogel computer**
  - Cell may be gate
  - Cell may be memory
  - Is space for cooling, but no cooling
- **Model application runtime**
- **Engineer real computer**
- **Model application runtime**
- **If runtimes similar, you succeeded**
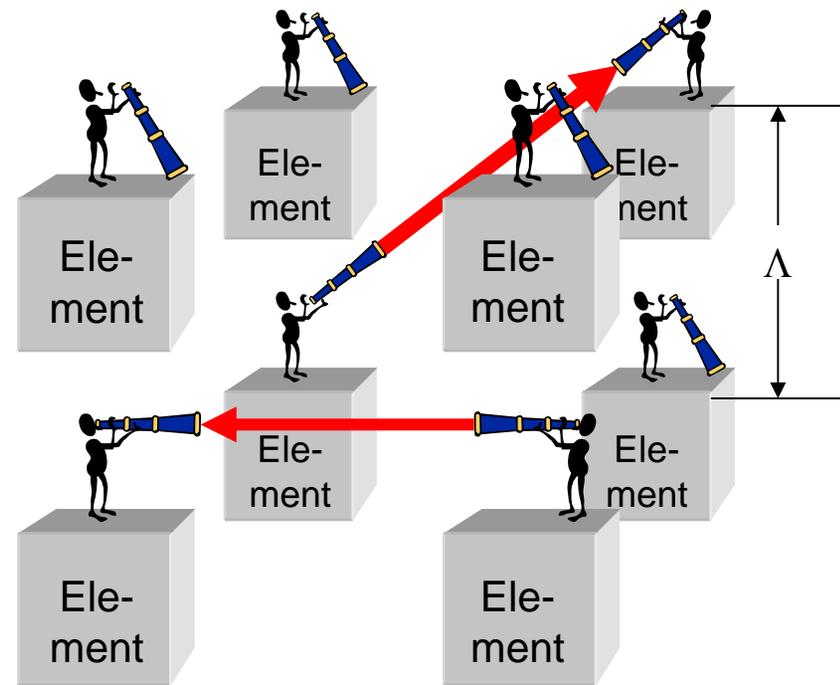
Element = Bit of memory or part of logic gate (transistor)

Aerogel Cooling

- **Inflate aerogel computer to point where heat emerging from faces is less than capacity of a designated cooling system**

  - **Air 45KW/m^2**

  - **Water 62MW/m^2**

  - **Pulse ∞W/m^2**

Inlet   Outlet

Inflated aerogel cooled from all six faces

Pyramid Structure:
$A_{in} + A_{out} = 6\,L_{Edge}^2$

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Architecture Target

Neighbors
in Mesh

ALU/FPU that
Evaluates Laws of
Physics at Max
Efficiency:
Signal Processor

Cell State Storage
for K Cells With
Max Efficiency
Access for Only
The Needed
Access Pattern

Neighbors
in Mesh

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Global Synchronization

Gather Dimension 1

Gather Dimension 2

Gather Dimension 3

Termination Decision & SOR Control (HOST)

Application Modeling

- **Sample Problem**
  - **3D finite difference equation with global synchronization**
  - **SOR method**

$$T_{Step} = \frac{K \times F_{cell}}{floprate} + T_{Global}$$

  - **where**
    - **K is memory size**

- **Global synchronization limited by speed of light**

$$T_{Global} \geq \frac{2\sqrt{3} \times L_{Edge}}{c}$$

  - **where**
    - **L_{Edge} is edge dimension of cube**

$$6 \times L_{Edge}^2 \times C_x \leq Power$$

Actual Applications Modeling

- **Actual code was several hundred lines of C++**
- **Theoretical limit covered**
  - **Coolant**
- **Realistic covered**
  - **Layout on a 2D surface of a particular size**
  - **Heat sink limits**
  - **I/O bandwidth from chip**
  - **Coolant**

Performance on Sample Problem

Interpretation:
• There is a limit, but it is not in the range of concern
• Better cooling yields higher limit, but mostly out of the range of our concern

Legend:
Air Cooling
Water Cooling
Fractal Plumbing
Pulse (no cooling)
Thick=Realistic
Thin=Theoretical Limit

Computer Time per Simulated Timestep (Lower is Better)

Systolic Array

PIM

MPP

Uniprocessor

Memory/Node

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Cost Efficiency

Plotting TFLOPS/Operating Cost of
15¢/KWH (electric power) +
$1000/chip (capital cost) +
$12/ft^2/year (machine room space)

Water cooling is better – but not by much!

Legend:
Air Cooling
Water Cooling
Fractal Plumbing
Pulse (no cooling)
Thick=Realistic
Thin=Theoretical Limit

Systolic Array   PIM   MPP   Uniprocessor

Memory/Node

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Outline

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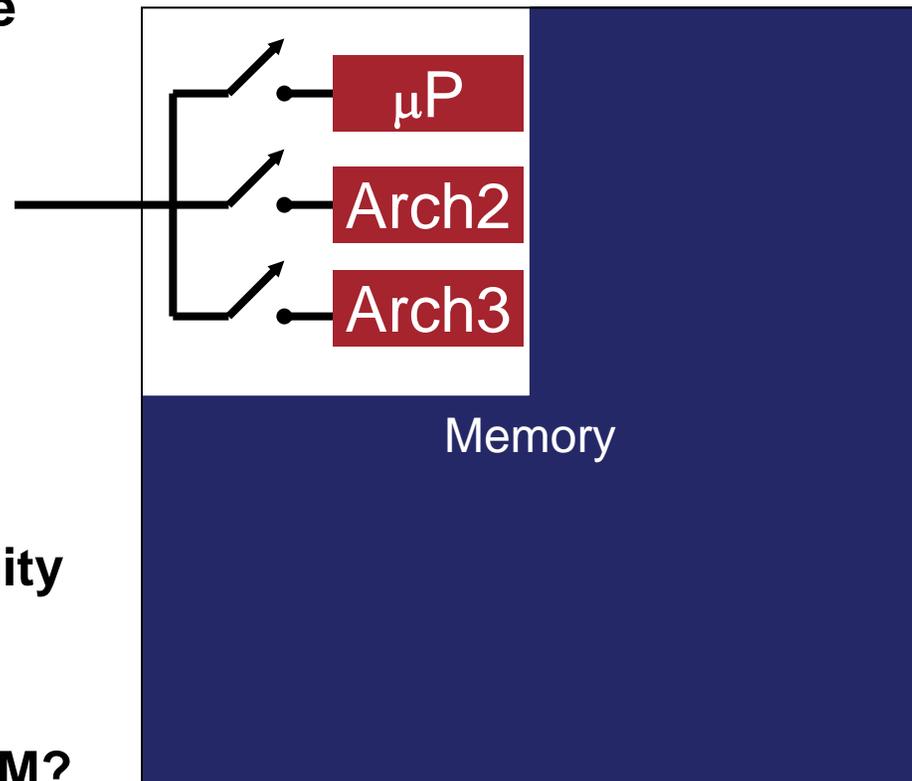- **No Need For a Breakthrough**
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Example of Computer at Physics Limit

- **Sandia is often approached by people who say we need some elaborate technology in order to run our applications at the Petaflops level**
  - Do we need elaborate technology?
  - Is the person just looking for research funding?
- **Question: can we make a computer that runs at the limits out of inexpensive components?**
  - Yes, subsequent slides are example

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Air-Cooled Packaging

Processor Array

Airflow

Air Conditioning Registers

Design minimizes signal travel distance while maximizing use of surface area for cooling
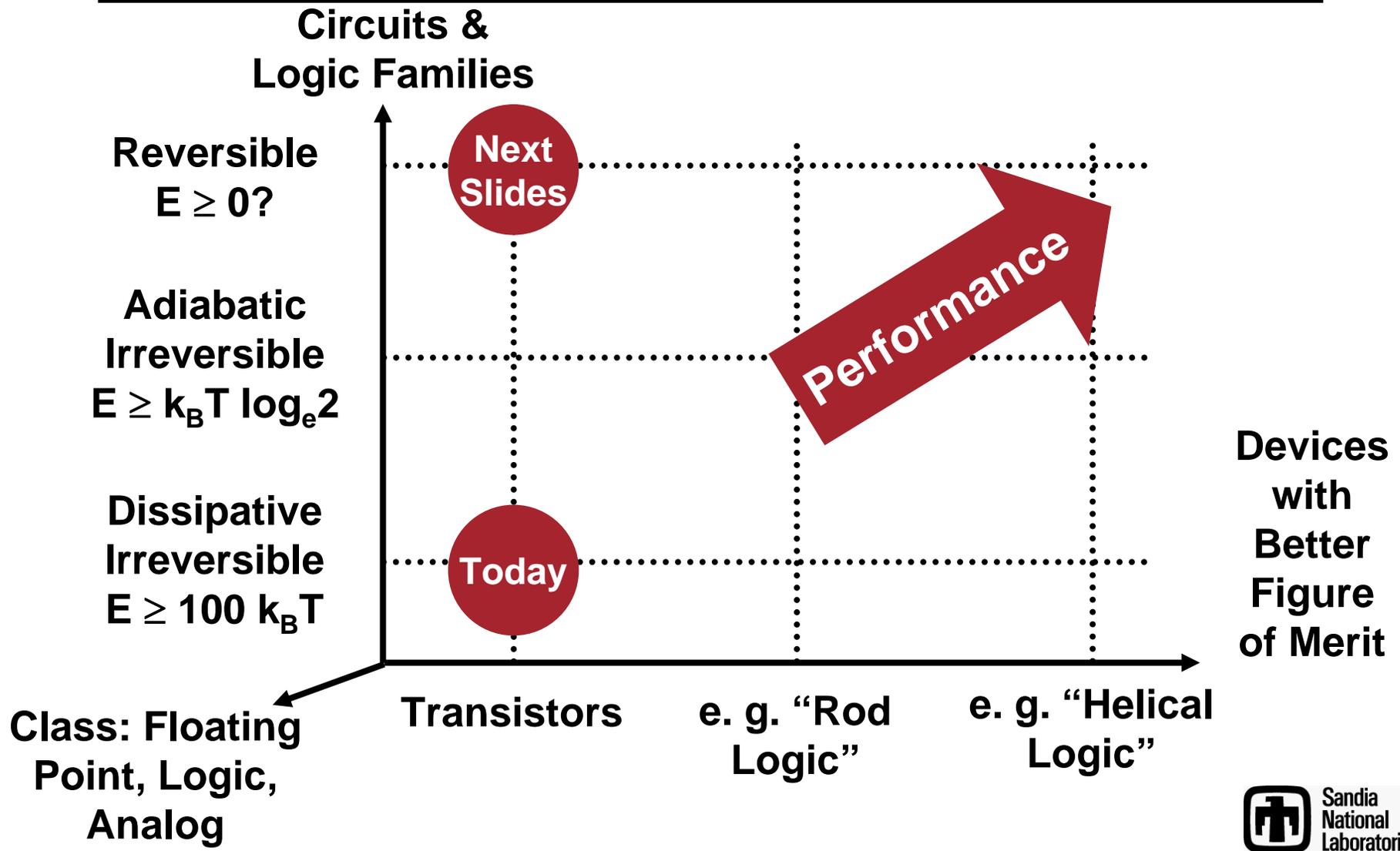
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Which Microarchitecture?

- Task: Pick a winner
  - Candidates μP, PIM, vector, FPGA, reconfigurable, streaming, maybe more
  - Each has advantages
  - Not clear which is best
  - Government gets bad press for picking winners too early

- Why do we pick winners
  - Logic is a scarce resource
  - But hang on a minute, don't we have more transistors than we know what to do with, and even turn some off at times?

- Can we change the rules of the game to make NOT picking a winner a virtue?

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Multi-Architecture Idea

- **Architecture to comprise**
  - μ**P and accelerator architectures 1 and 2**
  - **Power control circuit so only one is turned on at a time**
- **Benefit**
  - **Can expect support from cluster community and advocates of architectures 2 and 3**
- **Arch2=Vector, Arch3=PIM?**

Vdd

μP

Arch2

Arch3

Memory

Outline

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Beyond Moore's Law

Circuits & Logic Families

Reversible E $\geq$ 0?

Adiabatic Irreversible E $\geq k_B T \log_e 2$

Dissipative Irreversible E $\geq 100\ k_B T$

Class: Floating Point, Logic, Analog

(Next Slides)

(Today)

Performance

Devices with Better Figure of Merit

Transistors

e. g. "Rod Logic"

e. g. "Helical Logic"

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Reversible Logic

- **Reversible logic dissipates energy through "friction"**

- **If you run reversible logic at speed $\propto$ 1/n, it will dissipate power $\propto 1/n^2$**

- **However, any design will have a parasitic power loss, so actual loss is not $\propto 1/n^2$, but**

$$\text{Power} = \frac{P_0}{n^2} + P_{parasitic}$$

- **Measured power down 4$\times$, limit 2000$\times$**

Reversible Multiplier Status

- **8×8 Multiplier Designed, Fabricated, and Tested by IBM & University of Michigan**
- **Power savings was up to 4:1**

Reversible Microprocessor Status

- **Status**
  - **Subject of Ph. D. thesis**
  - **Chip laid out (no floating point)**
  - **RISC instruction set**
  - **C-like language**
  - **Compiler**
  - **Demonstrated on a PDE**
  - **However: really weird and not general to program with +=, -=, etc. rather than =**

Reversible Computer Engineering and Architecture

Carlin Vieri
MIT Artificial Intelligence Laboratory

Tom Knight: Committee chairman
Gerald Sussman, Gill Pratt readers
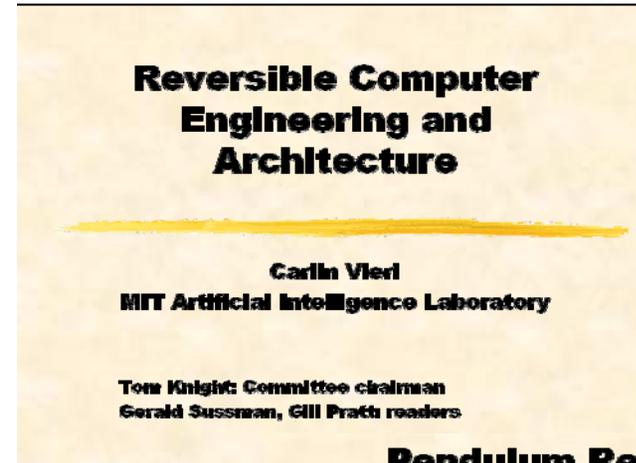
Pendulum Reversible Processor

Pendulum Chip

- 200,000 Transistors
- 18 Instructions
- 3-phase SCRL
- 50 mm^2 in HP14
- 180 Pins
  - 32 power supplies
- 2 Person years for schematics and layout

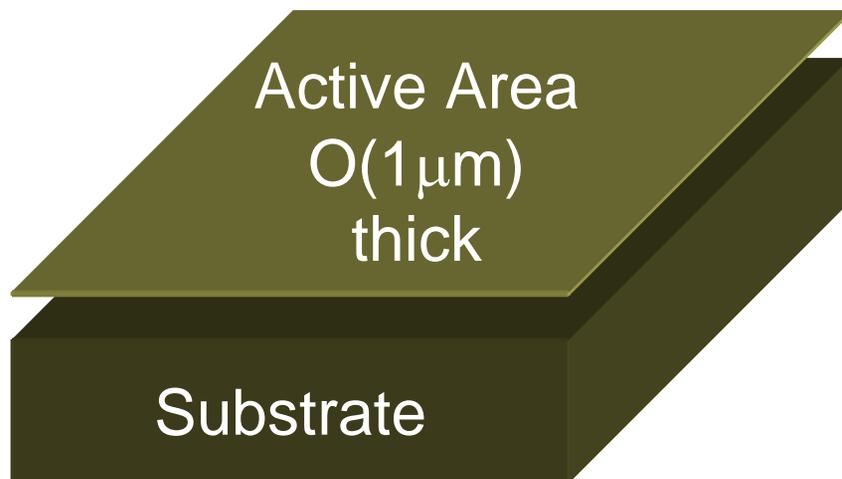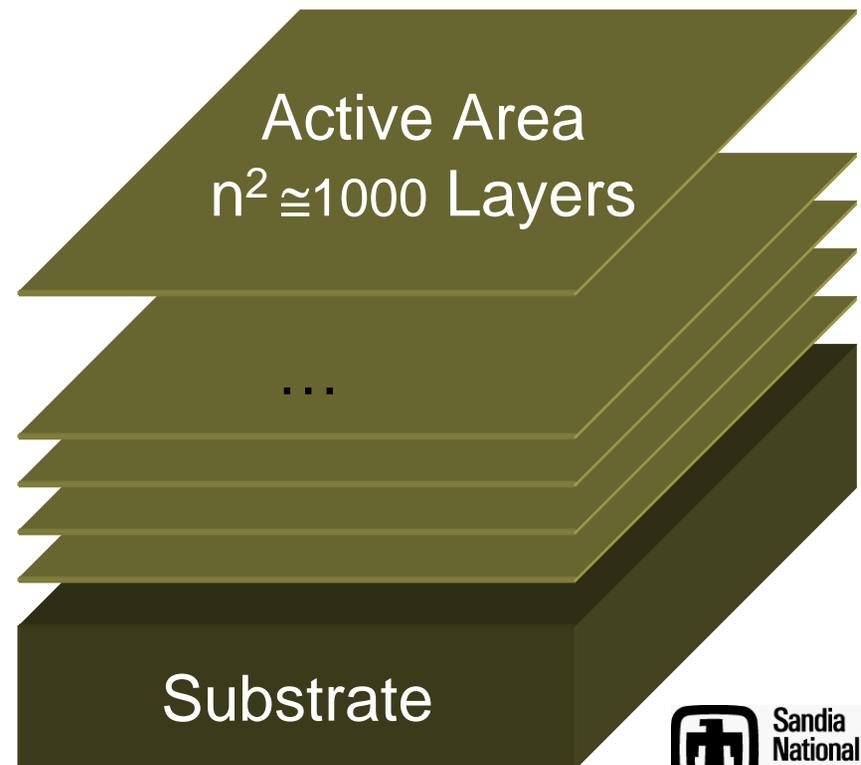# Thought Model for Reversible Red Storm

- **Replace each Red Storm node with chips constructed from $n^2 \cong 1000$ layers of reversible logic operating $1/n \cong 1/30$ speed**
- **Overall system $30\times$ faster, same power, $1000\times$ nodes**

- **Will become feasible for small "line width"**

Active Area
O(1μm)
thick

Substrate

Active Area
$n^2 \cong 1000$ Layers

...

Substrate

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Thought Model for Reversible Red Storm

	Conventional Logic Red Storm	Reversible n=30 Red Storm
Nodes	10,000	10,000,000
FLOPS/node	4 Gigaflops	100 Megaflops
Total FLOPS	40 Teraflops	1 Petaflops

Summary

- **Applications based on "simulating physics on a computer" scale up quite a ways**
  - Gave one example at 1 Exaflops & 1 Zetaflops
- **Semiconductor roadmap comes pretty close to physical limits for current class of computers**
  - Had chart with numerical FLOPS targets
  - Microprocessors cost about 100×
- **Other classes of computers are possible, but introduce disruptive change**

Ideas for Future Work

- **For computer architecture and software**
  - **Show scalability to the physical limits, but not beyond**
- **Estimate FLOPS for important problems to society that can be solved with computers**
  - **Which will be solvable with a computer of the current class, but scaled by Moore's Law?**
  - **Which will require a new class of computer?**
    - **These problems create a mandate for research into new classes of computer**

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Backup
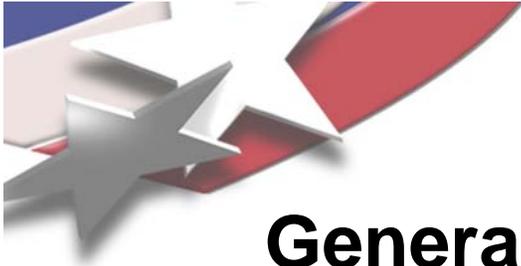
General Specifications at Physics Limit

	Red Storm	Limit μP Mode	Limit Turbo Mode
Nodes	10,000	200,000	2,000,000
Node Type	μP	μP	TBD – say 10 vector pipes
Clock	2 GHz	20 GHz	20 GHz
Flops/node	4 GFLOPS	40 GFLOPS	400 GFLOPS
Sys. Peak	40 TFLOPS	8 PFLOPS	800 PFLOPS
MPI Latency	2.5 μS	100 ns	N/A – no MPI
Power	2 MW	2 MW	2 MW

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The Cost of Beating Moore's Law

- A "1" and "0" must have more than 100× the thermal energy to avoid errors
    - Lowering the temperature doesn't help, it just shifts power to the refrigerator
- Today's irreversible logic destroys "1"s and "0"s at each gate. However, "reversible computing" recycles the energy in "1"s and "0"s. There is no known limit to "reversible computing."
- Quantum computing offers the possibility of exponential speedups

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Packaging for a Spatial Locality

- **Basic Module**
  - **2 Nodes**
  - **Each node is an ASIC System On Chip Processor In Memory**
  - **Each node has memory under ASIC**
  - **Each module includes a power module**
  - **Six mesh Interconnects**
- **Modules connect end-to-end in "Shish Kabobs"**

SOC PIM

Power Module

Memory
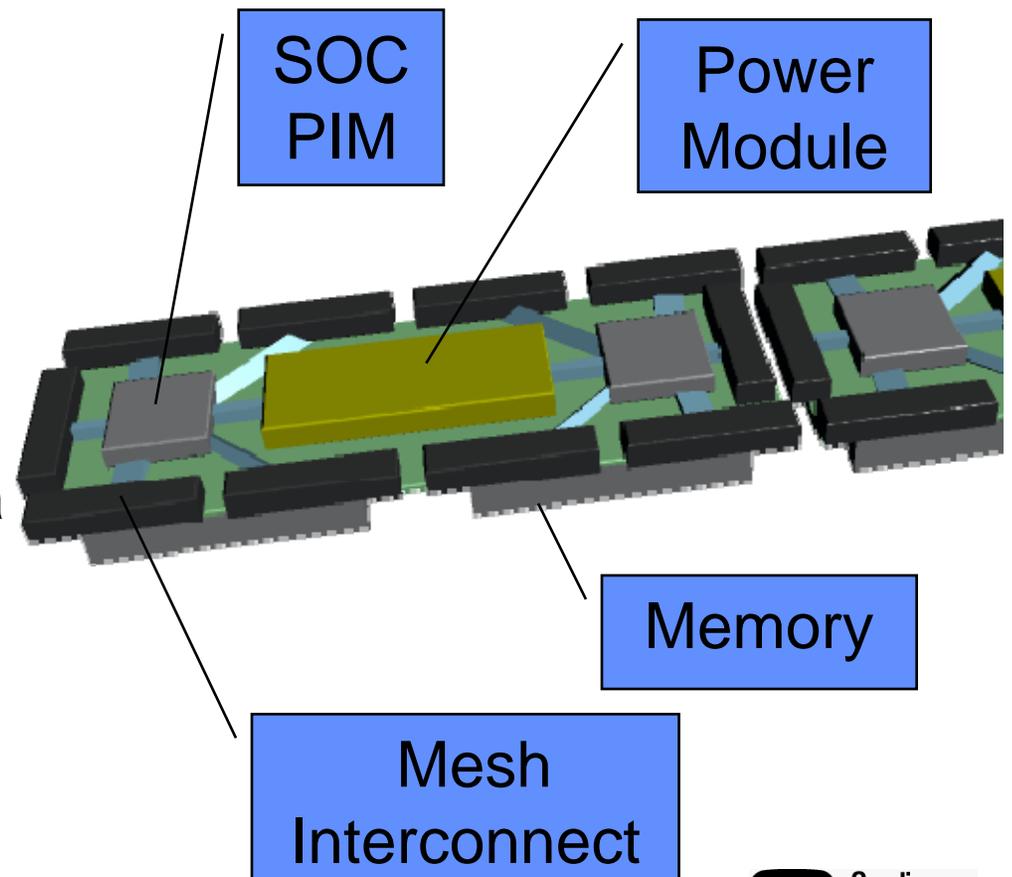
Mesh Interconnect

Packaging for a Spatial Locality

- **Entire supercomputer is a single structure**
- **All mesh network wires are of constant length (8" max)**
- **Air flows front to back**
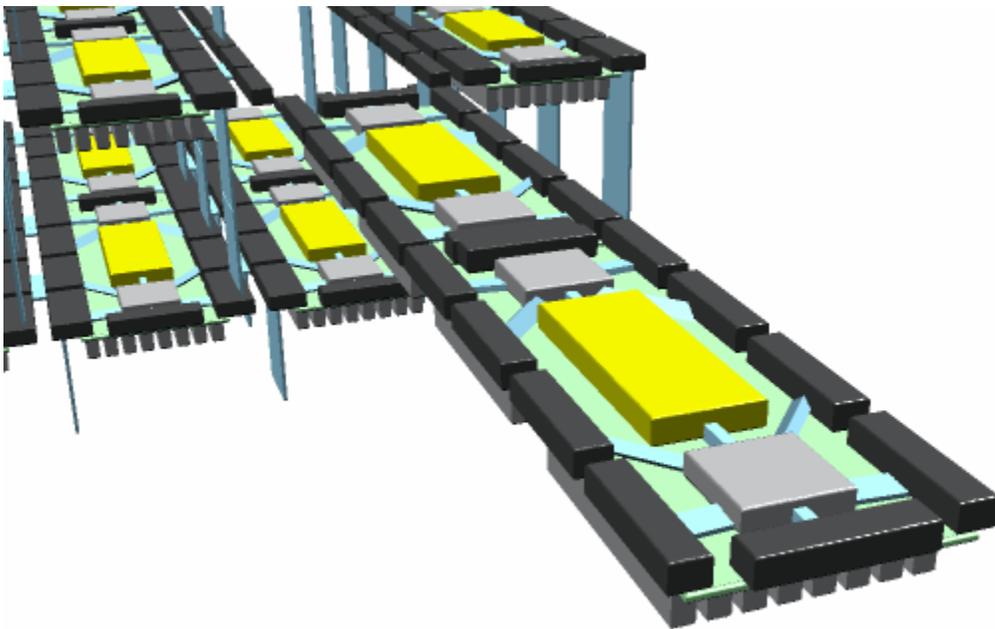 - **General approach will work for liquid cooling as well**

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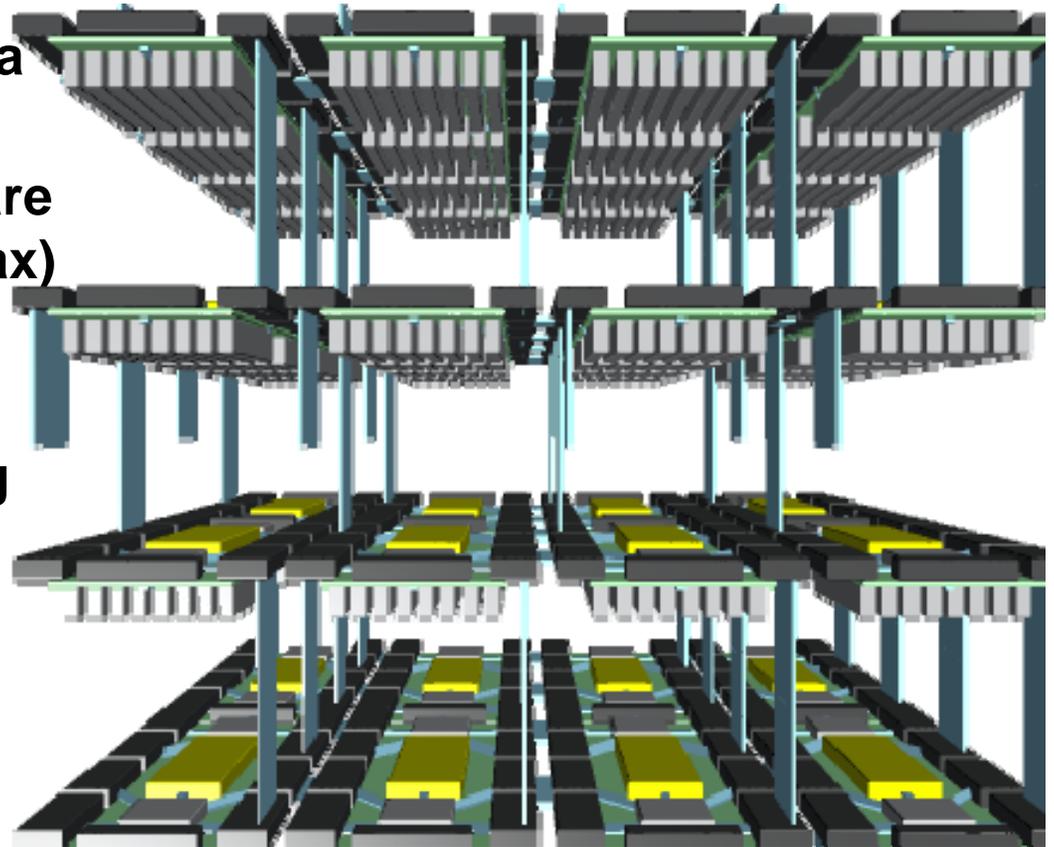
Nearest-Neighbor Interconnect

- **X Dimension**
  - **From one board to another laying in the same plane – 2"**
- **Y Dimension**
  - **8" from one board to another spaced above or below – 8"**
- **Z Dimension**
  - **Along the Shish Kabob – 4"**
  - **Name courtesy Monty Denneau IBM**
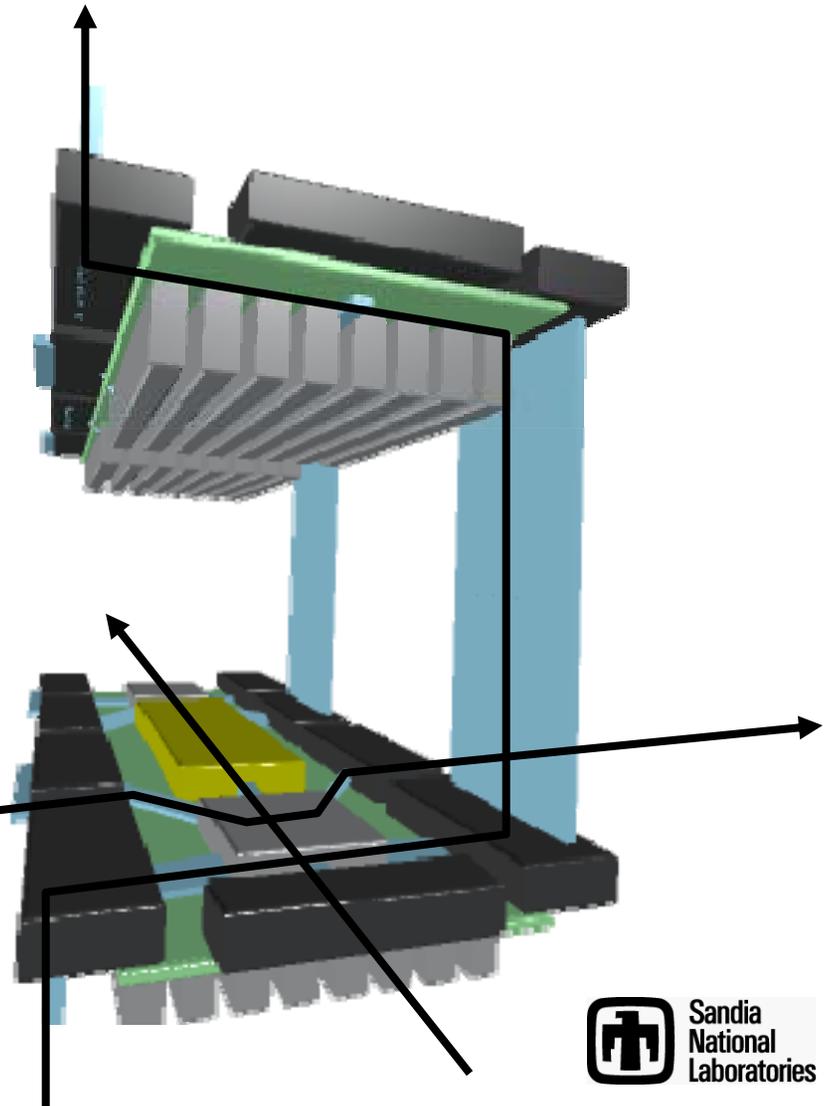
Maintenance

- Each "Shish Kabob" can be removed for maintenance
- Connects via side-connect technology
  - Similar to Cray shuttle connectors on T3E and X1
- Each Shish Kabob can be composed of segments to avoid limits on PC board technology
- Depth should be OK to 6'

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Backup: Landauer's Arguments

- **Landauer makes three arguments in his 1961 paper**
  - Kintetics of a bistable well
  - Entropy generation
- **We review the second →**

- **Entropy of a system in statistical mechanics:**

$$S = k_B \log_e(W)$$

  W is number of states

- **Entropy of a mechanical system containing a flip flop in an unknown state:**

$$S = k_B \log_e(2W)$$

- **After clearing the flip flop:**

$$S = k_B \log_e(W)$$

- **Difference $k_B \log_e(2)$**

Backup: Landauer's Arguments II

- **Second law of thermodynamics says entropy of universe must increase**
  - **Entropy is disorder**
- **Say you clear a computer memory of n bits. The computer's memory is initially disordered (arbitrary bits) but becomes ordered (all zero). Entropy goes down.**

- **However, entropy of universe must increase.**
- **Resolution is that the material of the memory chip becomes more disordered (hotter), offsetting the information in the memory**
- **A logic gate with multiple inputs but one output has fewer output states than input states: same idea**

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Backup: k_BT Should Not Be A Surprise

This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function.
– R. Landauer 1961

kT "helper line," drawn out of the reader's focus because it wasn't important at the time of writing
– Carver Mead, Scaling of MOS Technology, 1994
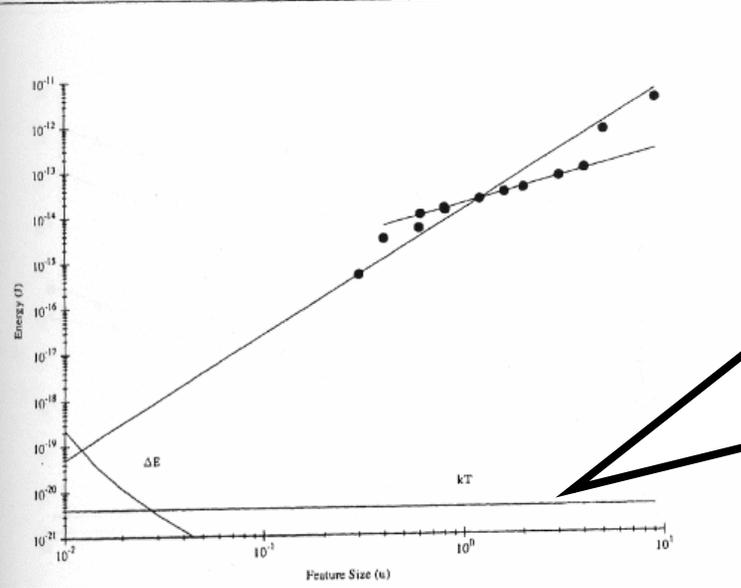
SCALING OF MOS TECHNOLOGY   97

Backup: Floating Point

- **A floating point unit has about 100,000 gates**
- **About 20,000 gates will switch for each operation**
- **Therefore,**

$$E_{FLOP} \approx$$
$$20,000 \; E_{gate} \approx$$
$$2,000,000 \; k_B \; T$$

- **Landauer limit is:**

   **100 TFLOPS/watt**

- **Accounting for engineering losses, more realistic:**

    10 TFLOPS/watt

- **If a μP is 1% efficient, the probable limit for a microprocessor is:**

    10 TFLOPS/watt chip
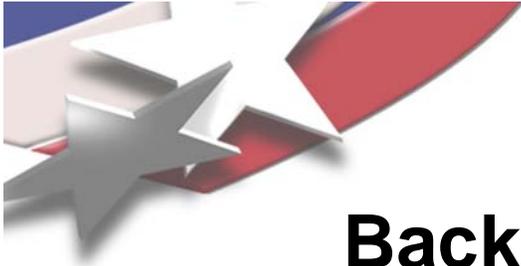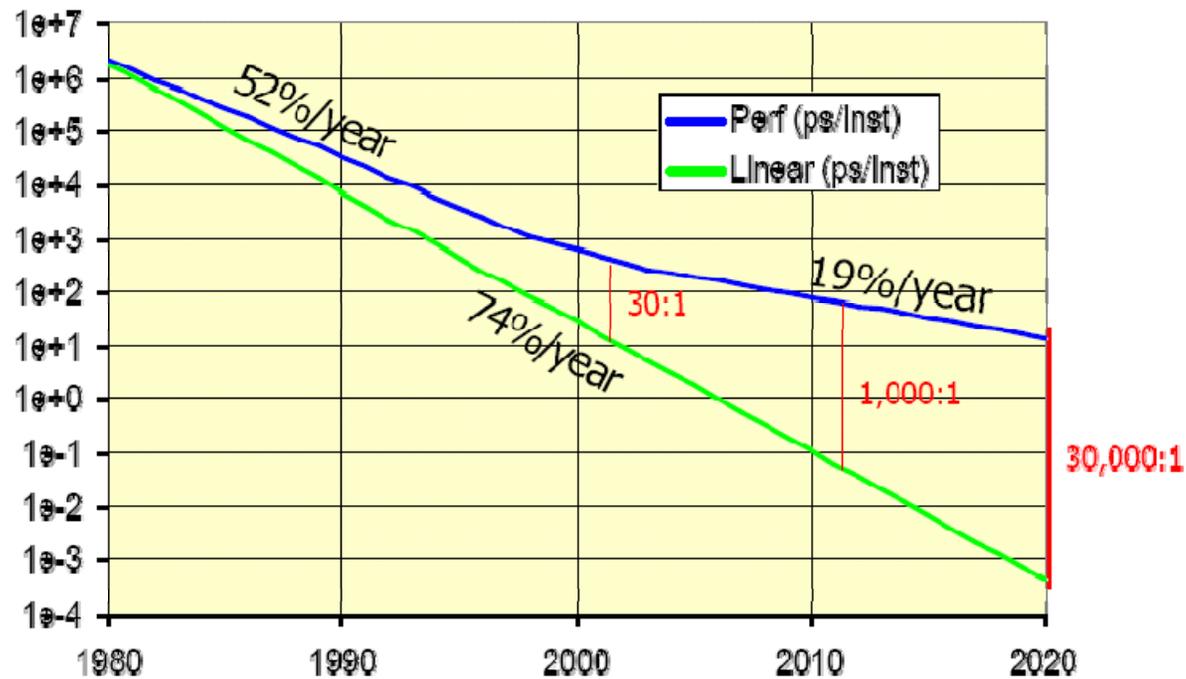
Backup: What About Cryogenics?

- **Minimum power per logic op 100 k_BT**
- **Minimum power per FLOP 2×10^6 k_BT**
- **Analysis**
  - At any T, performance may depend on cooling
  - Cutting T won't save power because of offsetting power in refrigerator, but may make cooling system more efficient
- **However**
  - Applications modeling indicates DOE apps aren't especially dependent on cooling
- **Conclusion: Use room temperature**
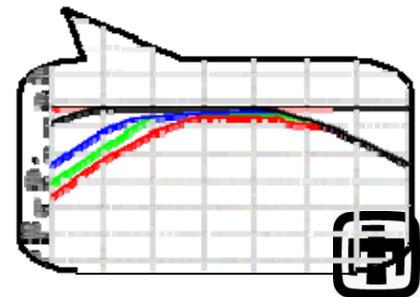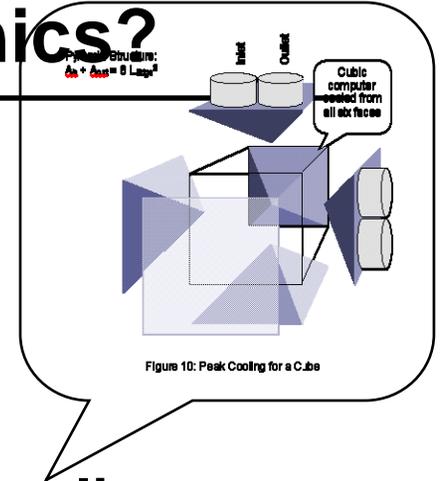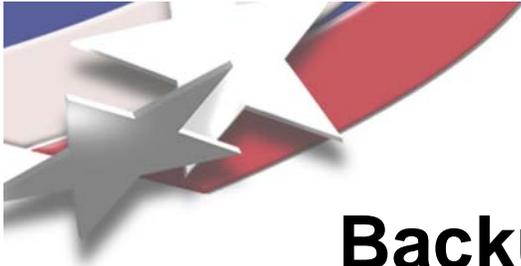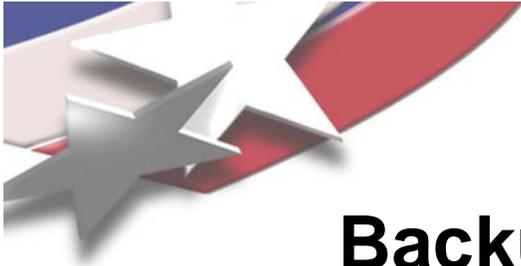
Figure 10: Peak Cooling for a Cube

Backup: Authority on μP Efficiency

Data parallelism realizes full potential of increased transistor count
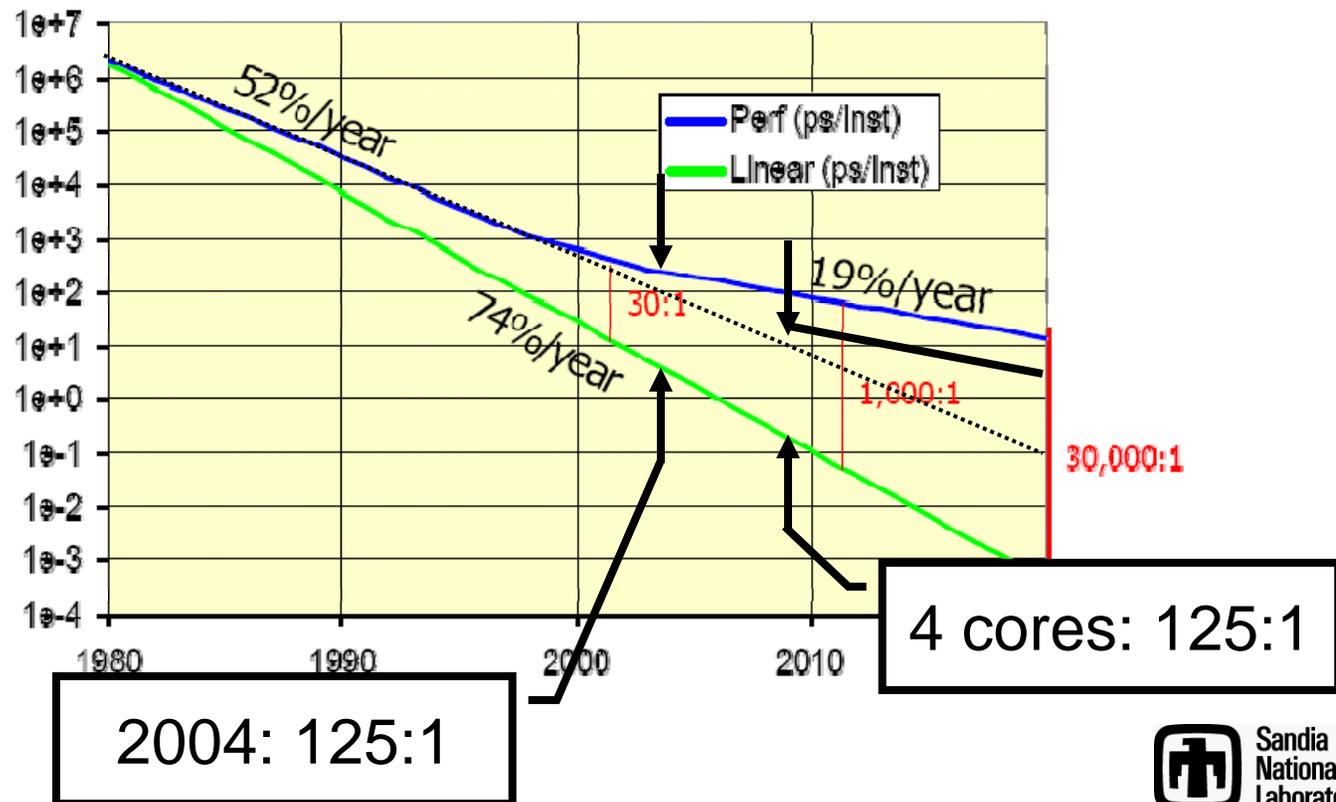

Citation:
Bill Dally,
ASCI PI
Meeting 2004

Backup: Authority on μP Efficiency

Data parallelism realizes full potential of increased transistor count

Citation:
Bill Dally,
ASCI PI
Meeting 2004

2004: 125:1

4 cores: 125:1

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March 6, 2004

Backup: Languages

- For many years, computer languages have targeted higher programmer productivity, trading easy programming for higher resource consumption during execution. This was believed to be OK because Moore's Law would cut the excess cost over time. Not so anymore

- Need to study languages for mature "irreversible logic" computers that are both easy to use and avoid excessive use of resources
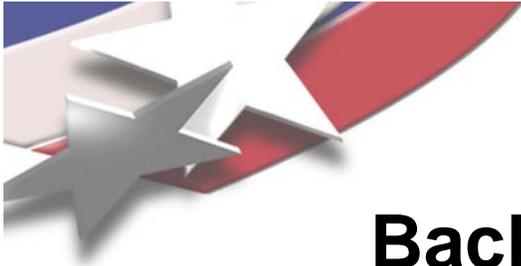
Backup Slide: Analog Computing

- **Floating Point Energy/Op**
  - $20{,}000 \times 100 \times k_B T =$
  - $2 \times 10^6 \; k_B T$
- **Analog Energy/Op**
  - $k_B T \log_e(\text{"\# states"})$
  - $k_B T \log_e(2^{64})$
  - $64 \; k_B T \log_e 2$
  - $44 \; k_B T$

- **Analog 45,000 more efficient**

- **Heisenberg Uncertainty Principle**
  - $\Delta E \; \Delta t \geq h/(2\pi)$
- **Waiting Time**
  - $\Delta E = 2^{-64} \times 64 \; k_B T \log_e 2$

  - $\Delta t \geq \dfrac{h}{2\pi \times 2^{-64} \times 64 \; k_B T \log_e 2}$

  - $\Delta t \geq \sim 3$ hours

- **Analog really slow**